

What is claimed is:

1 1. A trench capacitor` process for preventing
2 parasitic leakage, comprising the steps of:
3 providing a substrate with a trench formed therein,
4 wherein the trench has a buried plate formed
5 adjacent to the lower portion thereof;
6 forming a dielectric layer and a first conductive layer
7 in the lower portion of the trench, wherein the
8 buried plate and the first conductive layer are
9 separated by the dielectric layer;
10 forming a doping layer on portions of each sidewall of
11 the trench exposed by the dielectric layer and the
12 first conductive layer to reveal portions of
13 sidewalls of the trench in the upper portion;
14 forming a cap layer on each exposed sidewall and each
15 doping layer;
16 performing an annealing process on each doping layer to
17 forming a dopant region in the adjacent substrate,
18 wherein each dopant region blocks leakage current
19 resulted from a parasitic transistor adjacent to
20 the trench and has a first distance from the
21 surface of the substrate;
22 forming a second conductive layer in the trench to
23 expose portions of the cap layers, wherein the
24 second conductive layer contacts the first
25 conductive layer and has substantially the same
26 height with respect to the dopant regions;
27 removing portions of the cap layers exposed by the
28 second conductive layer to reveal portions of the
29 sidewalls in the upper portion of the trench; and

30 forming a third conductive layer on the second
31 conductive layer to fill the trench, wherein the
32 third conductive layer directly contacts the
33 exposed sidewalls in the upper portions of the
34 trench.

1 2. The trench capacitor process as claimed in claim
2 1, wherein the substrate is a p-substrate.

1 3. The trench capacitor process as claimed in claim
2 1, wherein the dielectric layer is nitride material.

1 4. The trench capacitor process as claimed in claim
2 3, wherein the nitride material is silicon nitride.

1 5. The trench capacitor process as claimed in claim
2 1, wherein the buried plate is an n-doped region in the
3 substrate adjacent to the lower portion of the trench.

1 6. The trench capacitor process as claimed in claim
2 1, wherein the first conductive layer, the second conductive
3 layer and the third conductive layer are n-doped
4 polysilicon.

1 7. The trench capacitor process as claimed in claim
2 6, wherein the n-doped polysilicon is arsenic-doped
3 polysilicon.

1 8. The trench capacitor process as claimed in claim
2 1, wherein the doping layer is boro-silicate-glass (BSG).

1 9. The trench capacitor process as claimed in claim
2 1, wherein the cap layer is silicon dioxide.

1 10. The trench capacitor process as claimed in claim
2 1, wherein the doping region is vertically distributed in
3 the substrate adjacent to the trench and approximately
4 equidistant from the trench.

1 11. The trench capacitor process as claimed in claim
2 1, wherein the annealing process is furnace annealing or
3 rapid thermal annealing (RTA).

1 12. The trench capacitor process as claimed in claim
2 1, wherein the charging conductivity of the dopants in the
3 doping region is the same as in the substrate.

1 13. The trench capacitor process as claimed in claim
2 1, wherein the concentration of the dopants in the doping
3 region is about double that in the substrate.

1 14. The trench capacitor process as claimed in claim
2 1, wherein the first distance is about 500~2500Å.

1 15. A trench capacitor process for preventing
2 parasitic leakage, capable of blocking leakage current
3 resulting from a parasitic transistor adjacent to the
4 trench, comprising the steps of:

5 forming a doping layer and a cap layer covering part of
6 the sidewall of the trench; and

7 performing an annealing process on the doping layer and
8 forming a dopant region in the substrate adjacent
9 to the sidewall of the trench to block leakage
10 current resulting from a parasitic transistor
11 adjacent to the trench.

1 16. The trench capacitor process as claimed in claim
2 15, wherein the doping layer is boro-silicate-glass (BSG).

1 17. The trench capacitor process as claimed in claim
2 15, wherein the cap layer is silicon dioxide.

1 18. The trench capacitor process for preventing
2 parasitic leakage as claimed in claim 15, wherein the
3 charging conductivity of the dopants in the doping region is
4 the same as that in the substrate.

1 19. The trench capacitor process as claimed in claim
2 15, wherein the concentration of the dopants in the doping
3 region is about double that in the substrate.

1 20. The trench capacitor process as claimed in claim
2 15, wherein the dopant region does not contact the surface
3 of the substrate and has a first distance therebetween.

1 21. The trench capacitor process as claimed in claim
2 20, wherein the first distance is about 500~2500Å.

1 22. A trench capacitor structure with an adjacent
2 parasitic leakage channel comprising:

3 a node diffusion and a buried well in the substrate
4 adjacent to a trench capacitor as a source or
5 drain region;

6 a dual-layered dielectric layer on a sidewall of the
7 trench capacitor as a gate dielectric and
8 electrically contacting the node diffusion and the
9 buried well;

10 a conductive layer on the dielectric layer to form a
11 parasitic transistor adjacent to the trench
12 capacitor;
13 a parasitic leakage channel of the parasitic transistor
14 in the substrate between the node diffusion and
15 the buried well; and
16 a dopant region in the substrate between the node
17 diffusion and the buried well to elevate a
18 threshold voltage for turning on the parasitic
19 leakage channel.

1 23. The trench capacitor structure as claimed in claim
2 22, wherein the charging conductivity of the dopants in the
3 doping region is the same as that in the substrate.

1 24. The trench capacitor structure as claimed in claim
2 22, wherein the concentration of the dopants in the doping
3 region is about double that in the substrate.